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IMPROVED ACTIVE FAILSAFE DETECTION FOR DIFFERENTIAL RECEIVER CIRCUITS

BACKGROUND OF THE INVENTION

Technical Field of the Invention

The present invention relates generally to the field of integrated circuits and, more particularly, to a method, system and apparatus of failsafe detection for differential receiver circuits.

Background of the Invention

For data transmission it is important to have bus drivers and bus receivers that allow devices to communicate quickly, efficiently, and accurately. This data transmission may occur within a computer system, for example. One common technique for implementation of data transmission within a computer bus uses differential signaling technology to communicate between devices in a computer system. A variety of differential signaling standards exist, such as low voltage differential signaling (LVDS), high voltage differential signaling (HVDS) and

others. Of course, such differential signaling may also be used for other long distance data transmission.

Typically, a LVDS driver includes a current source that drives the differential pair lines in opposition to each other. The differential receiver has a high DC impedance, so that the majority of driver current flows across a termination resistor generating a voltage drop across the receiver input. When the driver switches, it changes the direction of current flow across the resistor, thereby creating a valid "1" or "0" logic state. To help ensure reliability, differential receivers may have a failsafe feature that helps to insure the output to be in a known logic state under certain fault conditions. These fault conditions can include open, shorted, or terminated receiver input.

In interface circuits, and receiver circuits in general, it is advantageous to be able to detect failure conditions on the bus and react appropriately. Open circuit faults in general can cause problems in interface systems, sending receivers into unknown or oscillating states and generally causing havoc in digital systems. Failsafe circuits seek to detect such fault conditions and reactively apply a known state to the receiver outputs. It is also desirable that such failsafe detection circuits be capable of signaling or setting a fault bit so that digital circuits may deal with the fault conditions in a manner appropriate for the specific application.

Although current failsafe circuits are capable of accurately detecting/signaling on occurrence of the aforementioned fault conditions, they also signal false alarms in certain signal noise related events leading to uncertainty in the state of the receiver output.

SUMMARY OF THE INVENTION

The present invention achieves technical advantages as a method, system and apparatus for providing failsafe detection for a differential receiver. A bus activity signal is activated when receiving a differential data signal of sufficient amplitude to transition through a predetermined threshold. A failsafe signal is activated when a low differential voltage condition is detected. A countdown time period commences upon activation of either signal, and a failsafe condition is determined to exist if the failsafe signal is active when the countdown time period expires.

BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the present invention, reference is made to the following detailed description taken in conjunction with the accompanying drawings wherein:

Figure 1 illustrates a differential input stage circuit;

Figure 2 illustrates a simple circuit diagram of a failsafe type circuit used with the input stage circuit of Figure 1;

Figure 3 shows a graphical representation of an operation result of the failsafe type circuit shown in Figure 2;

Figure 4 shows a graphical representation of an invalid failsafe event which can occur when using the failsafe type circuit of Figure 2;

Figure 5 illustrates a method flow chart for failsafe detection in accordance with an embodiment of the present invention;

Figure 6 illustrates a failsafe circuit in accordance with an embodiment of the present invention;

Figure 7 shows a graphical representation of the output of the failsafe circuit shown in Figure 6; and

Figure 8 illustrates exemplary operations which can be performed by the embodiment of Figure 6.

DETAILED DESCRIPTION OF THE INVENTION

The numerous innovative teachings of the present application will be described with particular reference to the presently preferred exemplary embodiments. However, it should be understood that this class of embodiments provides only a few examples of the many advantageous uses and innovative teachings herein. In general, statements made in the specification of the present application do not necessarily delimit any of the various claimed inventions. Moreover, some statements may apply to some inventive features, but not to others.

Typical receiver architectures use one or more stages of low-gain/high-speed NPN input differential amplifiers to amplify an input signal, then a differential to single-ended converter stage to achieve rail-to-rail levels. Figure 1 illustrates the basic differential input stage architecture.

Referring to Figure 1, the differential pair Q1 and Q2 provide gain to the input signal at In1/In2. The emitters of Q1 and Q2 are respectively coupled to Vcc via resistors R1 and R2. Q3 and Q4 are connected as emitter followers, and act as level shifters to the input of the second stage. The level-shifted signal is taken from points A1/B1 to the input of the second stage. Resistors R3 and R4 create offset voltages which are proportional to the differential input voltage.

These voltages are used as inputs to a failsafe circuit. The second stage may include another amplification stage and a differential to single-ended converter, or may go directly to single ended conversion. After rail to rail levels are achieved, the second stage output goes directly into logic level gates as shown. A Timer Reset signal 11 is created from the logic level output of the receiver. The basic concept of the existing type failsafe circuit is to use window comparators to detect low differential voltage conditions on A1/B2 and B1/A2, and to use the Timer Reset signal to indicate bus activity.

Referring now to Figure 2 there is illustrated a simple circuit diagram of an existing failsafe type circuit that can be used with the input stage architecture shown in Figure 1.

In this circuit, window comparators 205, 210 are used to detect the differential voltage created by resistors R3 and R4 of Figure 1. When valid data exists at the inputs A2/B1, B2/A1, the outputs of one of the window comparators 205, 210 is high, and the other is low. When the differential input is below a predetermined level or threshold set by resistors R3 and R4 (from Figure 1), the outputs of both comparators are high. The output of the NAND gate 220, therefore, is high when there is valid data on the bus, and low when the data signal is below the failsafe threshold. The activity timer 230 keeps the failsafe bit

250 from triggering at every signal transition that takes the signal through the zone of an established threshold. The activity timer 230 monitors activity on the bus by taking the timer reset signal, from the circuit of Figure 1, as an input, and resets after a valid signal transition. In this way, the time required for invalid data to exist on the bus before a failsafe signal is issued can be set to a predetermined value. While there is bus activity of sufficient amplitude to drive the differential to single ended converter rail-to-rail, the output of the activity timer 230 is high. After activity has stopped, the activity timer 230 issues a low after a preset timeout period. After the activity timer 230 has gone low, the failsafe signal may go low (failsafe is active low) if a failsafe condition exists (NAND gate 220 output low) on the bus pins.

Referring now to Figure 3 there is illustrated a timing diagram which shows graphically the normal operation of the failsafe circuit illustrated in Figure 2. In this simulation, the two inputs 310, 320 are given a positive value indicating that valid data exists on a bus, then immediately brought to an invalid state below some predetermined positive failsafe threshold. After the valid data signal goes high, the failsafe signal 250 resets, then 800nS later (the failsafe timer setting in this simulation) failsafe is re-issued (Failsafe is active low).

One problem with the aforementioned failsafe circuit is that a failsafe can be issued due to noise during certain conditions, which can give false alarms, and set the receiver output in an incorrect state. One of the uses of the failsafe detection circuit is to set the state of the receiver output to a known state when a failsafe event is detected. This is accomplished by gating the receiver output with the failsafe signal. The problem occurs when valid data existing on the bus does not experience a signal transition in a time greater than the failsafe interval set by the activity timer 230. In this case, the output of the activity timer 230 is low, and failsafe output 250 of the OR gate 240 depends only on the NAND gate 220 output. If noise causes the differential voltage to momentarily dip below the predetermined failsafe threshold, the failsafe output 250 will immediately be activated. This happens because the activity timer 230 is only reset by the output of the receiver (timer reset signal from Figure 1), and not by the output of the window comparators 205, 210. Since, only a valid data transition resets the timer, false failsafe is introduced when, for example, the data signal experiences long periods of low in the presence of noise.

Referring now to Figure 4 there is illustrated an invalid failsafe event which occurs when using the failsafe circuit arrangement of Figure 2. In this illustration, inputs 410, 420 have been in a valid state above the receiver threshold for a period of time longer than the activity timeout period. A 10nS noise spike

on signal 420 causes a failsafe threshold detection followed by a failsafe (250) glitch low because the timeout period has expired. If the circuit in this example were connected such that the receiver output was gated high, for example, by the failsafe bit, the receiver output would have changed states without any valid data change on the input. Further, the receiver output can oscillate as noise dissipates and re-emerges.

Referring now to Figure 5 there is shown a method flow chart for exemplary failsafe detection for a differential receiver in accordance with the present invention. The method uses a timer which is configured for a predetermined timeout period 510. The timer is further configured to receive at least two reset input signals. The timeout period can be determined, by a designer, for a specific application. A differential data signal is monitored and compared to a predetermined receive threshold 520 for detecting a valid data transition of the differential data signal, and is compared to a failsafe threshold 530 for detecting a fault condition associated with the signal bus. Again, the predetermined receive and failsafe thresholds can be determined, by a designer, for a specific application. For each detected valid data transition and fault condition, a signal is enabled as an input to the timer, thus, resetting the timeout period 540. A failsafe bit or flag is set for a failsafe condition determined to persist subsequent to a timeout period. The failsafe bit or flag can then be used by

the differential receiver to deal with the fault condition in a manner appropriate for the specific application. The aforementioned method can be enabled in software, hardware or a combination of both.

Referring now to Figure 6 there is illustrated a failsafe circuit in accordance with an exemplary embodiment of the present invention. In this circuit, the activity timer 230 is reset for valid data transitions and data transitions which cross a predetermined failsafe threshold. Thus, the input to the activity timer 230 is toggled, by the XOR gate 640, whenever the Timer Reset switches (valid data transition) and whenever the window comparator 630 detects a failsafe threshold transition 620.

In the Figure 6 embodiment, comparators 205, 210 are used to detect differential voltage created by offset voltage resistors of a differential receiver device, such as R3 and R4 of Figure 1. The output of NAND gate 220 is high when there is valid data on the bus and low when the data signal is below a predetermined failsafe threshold. However, the output of the NAND gate 220 is delayed to OR gate 240 by a predetermined period. The delay device 650 is built into the OR gate input to keep a glitch or premature toggle from occurring when failsafe is detected. If the delay device 650 were not present, the failsafe condition would be transmitted through the OR gate 240 to the Failsafe bit at 660

before the activity timer 230 is reset, causing the glitch. The delay introduced by the delay device 650 must be longer than the inherent delay through the XOR gate 640 and the activity timer 230, such that the failsafe condition signaled by NAND gate 220 does not reach OR gate 240 before the activity timer output is driven high in response to the failsafe condition. The delay device 650 can be a simple RC circuit designed for a predetermined signal delay period.

Referring now to Figure 7 there is illustrated an output of a failsafe circuit in accordance with the present invention. The stimulus for the output shown in Figure 7 is the same stimulus as the illustration of Figure 4. The inputs 410, 420 have been in a valid state above the receiver threshold for a period of time longer than the activity timer 230 timeout period. The 10nS noise spike on signal 420 does not cause the failsafe 660 to glitch low as did failsafe 250 in Figure 4. When the circuit of Figure 6 is connected such that the receiver output is gated high by the failsafe bit, the receiver output does not change states on the occurrence of the noise spike unless the failsafe condition persist beyond the timeout period (which is reset on the occurrence of the depicted 10nS noise spike).

Referring now to Figure 8 there is illustrated exemplary operations which can be performed by the embodiment of Figure 6. The operations include determining if a valid data transition has occurred 81. If a valid data transition

has occurred, operation passes to commence a countdown time period 85, otherwise, operation passes to determining if a failsafe condition has occurred 82. From the failsafe condition determination operation 82, when a failsafe condition occurrence is determinative, operation again passes to commence a countdown time period 85, otherwise, operation passes to determine if the countdown period has expired 86. From the countdown period expiration determination operation 86, when an expiration is determinative, operation passes to determine if a failsafe condition is active 87, otherwise operation passes back to the valid data transition determination operation 81. From the failsafe condition active operation 87, a determinative active failsafe condition passes operation control to activate a failsafe flag 89, otherwise operation passes back to the valid data transition determination operation 81.

Although a preferred embodiment of the method and system of the present invention has been illustrated in the accompanied drawings and described in the foregoing Detailed Description, it is understood that the invention is not limited to the embodiments disclosed, but is capable of numerous rearrangements, modifications, and substitutions without departing from the spirit of the invention as set forth and defined by the following claims.